UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,335	06/11/2001	Vishnu K. Agarwal	MI22-1568	4063

21567 7590 05/21/2003

WELLS ST. JOHN ROBERTS GREGORY & MATKIN P.S.
601 W. FIRST AVENUE
SUITE 1300
SPOKANE, WA 99201-3828

EXAMINER
HUYNH, YENNHU B

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,335	AGARWAL ET AL.	
	Examiner	Art Unit	
	Yennhu B Huynh	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50 and 58-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50 and 58-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). ____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the RCE filed on 11/26/03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4, 5-8,13-19,21, 58-60 &16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gonzalez (U.S. 5,608,249).

Gonzales at figs. 1-8 in col. 1-10 disclose reduced area storage node junction, which include:

-Re. claims 1 & 16: forming an insulation layer 30 over substrate 12, the substrate include an electronic device transistor 18 (fig.1); forming a barrier layer 41 to shift inducing material over the substrate (figs. 4 & 5, col.6, line 24); forming an opening at least into the insulation layer (figs.1 & 2); forming a high K capacitor dielectric layer 46 at least within the opening (figs. 7 & 8, col.6, lines 60-63); and providing a threshold voltage shift inducing material over the barrier layer, the barrier layer retarding movement of the threshold voltage shift inducing material into the electronic device (col. 6, lines 24-30).

-Re. claims 2,4,18,58 & 60: wherein the barrier layer 41 is formed over the insulation layer 30 and planarized (figs. 1-6, col.6, lines 8-32) .

-Re. claims 3 & 17: wherein the barrier comprises of nitride (col.6, lines 9-14).

-Re. claim 5: wherein the forming an opening further comprises forming a congruent opening through the barrier layer (figs. 1-6).

-Re. claim 6: wherein the opening is formed completely through the insulation layer (figs. 2-8).

-Re. claims 7 & 19: wherein the dielectric layer comprises material with high dielectric constant, and Ta2O5 is a type of high dielectric constant (col.6, lines 60-63).

-Re. claims 8 & 59: wherein the threshold voltage shift material comprises providing at least one impurity comprising layer over the barrier layer an insulation layer (col.6, lines 24-29).

-Re.claim 13: wherein the electronic device comprises a transistor 18 (figs. 1-8).

-Re. claim 14: wherein the substrate comprises a bulk semiconductor wafer (col.1, lines 18-21).

-Re. claim 15: forming a capacitor electrode 44 at least within the opening before forming the dielectric layer 46 (figs. 6-8, col.6, lines 33-35 and 60-63).

-Re. claim 21: forming a capacitor electrode 44 within the opening before forming the dielectric layer (fig. 7).

(188) = Al = barrier = metal Nr. e.G = /

Claims 22-35 & 61-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Parekh et al. (U.S. 6,165,833).

Parekh et al. at figs. 1-7 in col. 1-6 disclose method of forming capacitor, which include:

-Re. claims 22 & 29: forming a barrier layer 25 to Vt inducing material over a substrate 12 include an electronic device 14 (col.4, lines 12-15); forming an insulation layer 32 over the barrier layer 25; forming an opening 34 into at least the insulation layer 32; forming a high K capacitor dielectric layer 42 at least within the opening 34; and providing Vt shift inducing material over the barrier layer and insulation, the barrier layer retarding movement of the Vt shift inducing material into the electronic device 14 (figs. 3-7, col. 3, lines 2-5 & 9-13 and col. 4 & 5, lines 12-3).

-Re. claims 23,24,30,31 & 61-64: wherein the barrier layer 25 is a silicon nitride, a planarized barrier layer, and formed on the substrate and insulation layer (figs. 3-6, col.4, lines 12-33).

-Re. claims 26 & 33: wherein the dielectric layer 42 comprises material with high dielectric constant Ta2O5 (col. 5, lines 4-6).

- Re. claims 27 & 34: wherein the providing Vt shift inducing material comprising oxide annealing the dielectric layer and nitride (col.4 & 5, lines 53-3 and col. 6, lines 25-33 & 40-46)

-Re. claims 28 & 35: forming a capacitor electrode 36 at least within the opening 34 before forming the dielectric layer 42 (col.4, lines 43-53).

-Re. claims 25 & 32: wherein the opening 34/56 is formed completely through the second insulation layer 32, barrier layer 25 and into the first insulation layer 26 by plug 28/30 (fig.7, col.5, lines 17-29).

37.2 C, 12, 14 G

Claims 36-50 & 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Thakur et al (U.S. 6,251,720B1).

Thakur et al. at figs.1-5 in col. 1-18 disclose a HDC capacitive dielectric film in capacitor, which include:

-Re. claims 36 & 43: forming an insulation layer 116 over substrate 101 including an electronic device 110 ; an opening into the insulation layer and having a sidewall (fig. 1A); a capacitor electrode 104 at least within the opening and over the sidewall; after forming the capacitor electrode, forming a barrier layer 122 (col.8) to Vt shift inducing material at least over the insulation layer; then forming a high K capacitor dielectric layer 102 at least over the insulation layer and capacitor electrode (col.8); providing Vt shift inducing material over the barrier layer to the electronic device (col. 8 & 9, lines 58-24).

-Re. claims 39, 47 & 65: wherein the barrier layer 122 comprises Si3N4 and formed on the insulation layer (col.5, lines 36-50).

-Re. claims 40 & 48: wherein the barrier layer is planarized in planarized the structure (col. 10, lines 12-14)

-Re. claims 41 & 44: wherein the dielectric layer 102 comprises Ta2O5 (col.10, lines 1 & 8-11).

-Re. claims 42 & 49: wherein annealing the dielectric with oxide and N2O (col. 10, lines 23-53)

-Re. claim 50: wherein annealing the dielectric and forming the barrier layer before the annealing structure (col. 10, lines 54-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-12 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez (U.S.5,608,249) in view of Tsunemine (U.S. 5,699,291).

Gonzaler disclose substantially all of claimed invention, except annealing the dielectric layer (cl.9); annealing with oxide and N2O (cls. 10 & 12); the heating treatment at least about 600 C degrees with nitrogen containing oxide and a partial pressure of about 200 mmTorr (cl.11). Tsunemine at figs. 1-19 in col.1-4 disclose a method of manufacturing semiconductor memory device, which include:

-Re. claims 9-12 & 20: wherein the providing Vt shift inducing material comprising oxide, N2O annealing the dielectric layer 102 , at least about 200-950 C degrees the

heating at least about 600 C degrees with nitrogen containing oxide and a partial pressure of about 1-25 atmospheres (col.10, lines 23-46).

It would have been obvious to one having skill in the art at the time the invention was made to modify the invention of Gonzalez by incorporating the dielectric annealing at a high temperature to densify the layer and prevent leakage current problem.

Claims 37,38,45 & 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thakur et al (U.S. 6,251,720B1)

Thakur et al. disclose substantially all of claimed invention, except for the barrier layer comprises CVD at step coverage of less than about 25% and thickness over the sidewall of from about 0-300 Angstrom.

With respect to claims 37,38,45 & 46 the time, concentration, dimension and thickness are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art, As noted In re Aller 105 USPQ233, 255 (CCPA 1955). The selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to expected that a change in temperature, or in range, concentration, cycles, thickness, would be an unpatentable modification. Under some circumstance, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ

372 (CPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yennhu Huynh whose telephone number is (703)308-6110. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4.30PM.

If attempts to reach the examiner by telephone are unsuccessfully, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

YNBH,

4/27/03

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800